Nonvolatile, I²C-Compatible 256-Position, Digital Potentiometer

AD5259

FEATURES

- Nonvolatile memory maintains wiper settings
- 256-position
- Thin LFCSP-10 (3 mm x 3 mm x 0.8 mm) package
- Compact MSOP-10 (3 mm × 4.9 mm x 1.1mm) package
- I²C®-compatible interface
- V_{LOGIC} pin provides increased interface flexibility
- End-to-end resistance 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
- Resistance tolerance stored in EEPROM (0.1% accuracy)
- Power-on EEPROM refresh time < 1ms
- Software write protect command
- Address Decode Pin AD0 and Pin AD1 allow 4 packages per bus
- 100-year typical data retention at 55°C
- Wide operating temperature −40°C to +85°C
- 3 V to 5 V single supply

APPLICATIONS

- LCD panel V_{COM} adjustment
- LCD panel brightness and contrast control
- Mechanical potentiometer replacement in new designs
- Programmable power supplies
- RF amplifier biasing
- Automotive electronics adjustment
- Gain control and offset adjustment
- Fiber to the home systems
- Electronics level settings

GENERAL DESCRIPTION

The AD5259 provides a compact, nonvolatile LFCSP-10 (3 mm × 3 mm) or MSOP-10 (3 mm × 4.9 mm) packaged solution for 256-position adjustment applications. These devices perform the same electronic adjustment function as mechanical potentiometers[1] or variable resistors, but with enhanced resolution and solid-state reliability.

The wiper settings are controllable through an I²C-compatible digital interface that is also used to read back the wiper register and EEPROM content. Resistor tolerance is also stored within EEPROM, providing an end-to-end tolerance accuracy of 0.1%.

A separate V_{LOGIC} pin delivers increased interface flexibility. For users who need multiple parts on one bus, Address Bit AD0 and Address Bit AD1 allow up to four devices on the same bus.

FUNCTIONAL BLOCK DIAGRAMS

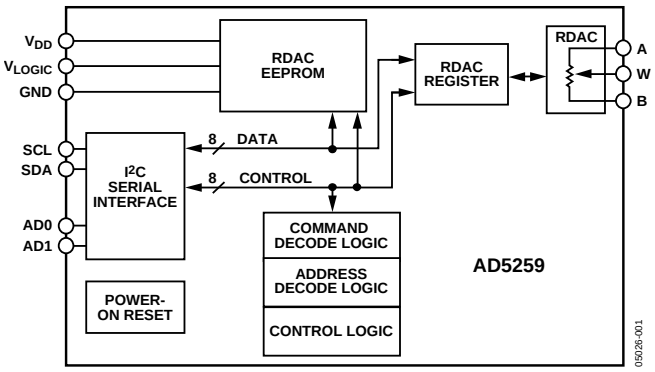

Figure 1. Block Diagram

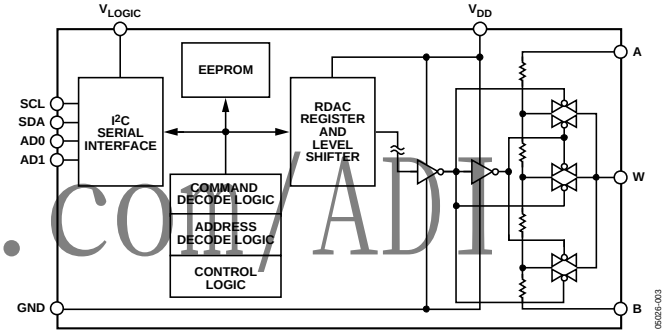

Figure 2. Block Diagram Showing Level Shifters

CONNECTION DIAGRAM

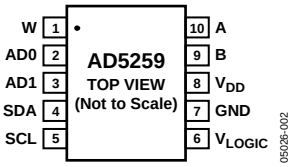

Figure 3. Pinout

[1] The terms digital potentiometer, VR (variable resistor), and RDAC are used interchangeably.

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TABLE OF CONTENTS

Specifications ... 3
Electrical Characteristics ... 3
Timing Characteristics ... 5
Absolute Maximum Ratings ... 6
ESD Caution ... 6
Pin Configuration and Function Descriptions ... 7
Typical Performance Characteristics ... 8
Test Circuits ... 13
Theory of Operation ... 14
Programming the Variable Resistor ... 14
Programming the Potentiometer Divider ... 14
I²C-Compatible Interface ... 15
Writing ... 15
Storing/Restoring ... 15
Reading ... 15
I²C-Compatible Format ... 16
Generic Interface ... 16
Write Modes ... 16
Read Modes ... 17
Store/Restore Modes ... 17
Tolerance Readback Modes ... 18
ESD Protection of Digital Pins and Resistor Terminals ... 19
Power-Up Sequence ... 19
Layout and Power Supply Bypassing ... 19
Multiple Devices on One Bus ... 19
Evaluation Board ... 19
Display Applications ... 20
Circuitry ... 20
Outline Dimensions ... 21
Ordering Guide ... 21

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REVISION HISTORY

7/05 — Rev. 0 to Rev. A

Added 10-Lead LFCSP ... Universal
Changes to Features Section and General Description Section ... 1
Changes to Table 1 ... 3
Changes to Table 2 and Added Figure 4 ... 5
Changes to Table 4 ... 7
Changes to Figure 27 Caption ... 11
Changes to Theory of Operation Section ... 14
Changes to I²C-Compatible Interface Section ... 15
Changes to Table 5 ... 16
Changes to Multiple Devices on One Bus Section ... 19
Updated Figure 49 Caption ... 21
Changes to Ordering Guide ... 21

2/05 — Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = V_{LOGIC} = 5 V ± 10% or 3 V ± 10%; V_A = V_{DD}; V_B = 0 V; −40°C < T_A < +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS: RHEOSTAT MODE						
Resistor Differential Nonlinearity	R-DNL	R_{WB}, V_A = no connect				LSB
5 kΩ			−1	±0.2	+1	
10 kΩ			−1	±0.1	+1	
50 kΩ/100 kΩ			−0.5	±0.1	+0.5	
Resistor Integral Nonlinearity	R-INL	R_{WB}, V_A = no connect				LSB
5 kΩ			−4	±0.3	+4	
10 kΩ			−2	±0.2	+2	
50 kΩ/100 kΩ			−1	±0.4	+1	
Nominal Resistor Tolerance	ΔR_{AB}	T_A = 25°C, V_{DD} = 5.5 V	−30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB} \times 10^6)/(R_{AB} \times \Delta T)$	Code = 0x00/0x80		500/15		ppm/°C
Total Wiper Resistance	R_{WB}	Code = 0x00		75	350	Ω
DC CHARACTERISTICS: POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity	DNL					LSB
5 kΩ			−1	±0.2	+1	
10 kΩ			−0.5	±0.1	+0.5	
50 kΩ/100 kΩ			−0.5	±0.2	+0.5	
Integral Nonlinearity	INL					LSB
5 kΩ			−1	±0.2	+1	
10 kΩ			−0.5	±0.1	+0.5	
50 kΩ/100 kΩ			−0.5	±0.1	+0.5	
Full-Scale Error	V_{WFSE}	Code = 0xFF				LSB
5 kΩ			−7	−3	0	
10 kΩ			−4	−1.5	0	
50 kΩ/100 kΩ			−1	−0.4	0	
Zero-Scale Error	V_{WZSE}	Code = 0x00				LSB
5 kΩ			0	2.5	4	
10 kΩ			0	1	3	
50 kΩ/100 kΩ			0	0.2	0.5	
Voltage Divider Temperature Coefficient	$(\Delta V_W \times 10^6)/(V_W \times \Delta T)$	Code = 0x00/0x80		60/5		ppm/°C
RESISTOR TERMINALS						
Voltage Range	$V_{A, B, W}$		GND		V_{DD}	V
Capacitance A, B	$C_{A, B}$	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		10		nA

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Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		0.7 × V_L		V_L + 0.5	V
Input Logic Low	V_{IL}		−0.5		0.3 × V_L	V
Leakage Current	I_{IL}					μA
SDA, AD0, AD1		V_{IN} = 0 V or 5 V		0.01	±1	
SCL – Logic High		V_{IN} = 0 V	−2.5	−1.3	+1	
SCL – Logic Low		V_{IN} = 5 V		0.01	±1	
Input Capacitance	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
Positive Supply Current	I_{DD}			0.1	2	μA
Logic Supply	V_{LOGIC}		2.7		5.5	V
Logic Supply Current	I_{LOGIC}	V_{IH} = 5 V or V_{IL} = 0 V		3	6	μA
Programming Mode Current (EEPROM)	$I_{LOGIC(PROG)}$	V_{IH} = 5 V or V_{IL} = 0 V		35		mA
Power Dissipation	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V		15	40	μW
Power Supply Rejection Ratio	PSRR	V_{DD} = +5 V ± 10%, code = 0x80		±0.005	±0.06	%/%
DYNAMIC CHARACTERISTICS						
Bandwidth −3 dB	BW	Code = 0x80				
		R_{AB} = 5 kΩ		2000		kHz
		R_{AB} = 10 kΩ		800		kHz
		R_{AB} = 50 kΩ		160		kHz
		R_{AB} = 100 kΩ		80		kHz
Total Harmonic Distortion	THD_W	R_{AB} = 10 kΩ, V_A = 1 V rms, V_B = 0, f = 1 kHz		0.01		%
V_W Settling Time	t_S	R_{AB} = 10 kΩ, V_{AB} = 5 V, ±1 LSB error band		500		ns
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		9		nV/√Hz

[1] Typical values represent average readings at 25°C and V_{DD} = 5 V.

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TIMING CHARACTERISTICS

$V_{DD} = V_{LOGIC} = 5\ V \pm 10\%$ or $3\ V \pm 10\%$; $V_A = V_{DD}$; $V_B = 0\ V$; $-40°C < T_A < +85°C$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C INTERFACE TIMING CHARACTERISTICS[1]						
SCL Clock Frequency	f_{SCL}		0		400	kHz
t_{BUF} Bus Free Time Between Stop and Start	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6			µs
$t_{SU;STA}$ Setup Time for Repeated Start Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6		0		0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for Stop Condition	t_{10}		0.6			µs
EEPROM Data Storing Time	t_{EEMEM_STORE}			26		ms
EEPROM Data Restoring Time at Power On[2]	$t_{EEMEM_RESTORE1}$	V_{DD} rise time dependent. Measure without decoupling capacitors at V_{DD} and GND.		300		µs
EEPROM Data Restoring Time upon Restore Command[2]	$t_{EEMEM_RESTORE2}$	$V_{DD} = 5\ V$.		300		µs
EEPROM Data Rewritable Time[3]	$t_{EEMEM_REWRITE}$			540		µs
FLASH/EE MEMORY RELIABILITY						
Endurance[4]			100	700		kCycles
Data Retention[5]				100		Years

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[1] Standard I²C mode operation guaranteed by design.
[2] During power-up, the output is momentarily preset to midscale before restoring EEPROM content.
[3] Delay time after power-on PRESET prior to writing new EEPROM data.
[4] Endurance is qualified to 100,000 cycles per JEDEC Std. 22 method A117, and is measured at –40°C, +25°C, and +85°C; typical endurance at +25°C is 700,000 cycles.
[5] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.

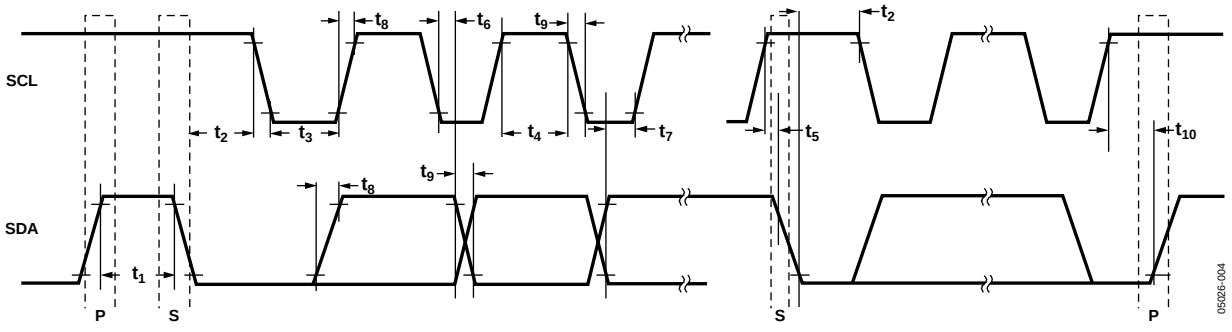

Figure 4. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Value
V_{DD}, V_{LOGIC} to GND	−0.3 V to +7 V
V_A, V_B, V_W to GND	GND − 0.3 V, V_{DD} + 0.3 V
I_{MAX}	
Pulsed[1]	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[2]	
θ_{JA}: MSOP−10	200°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = (T_{JMAX} − T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

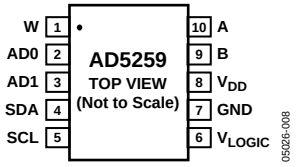

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin	Mnemonic	Description
1	W	W Terminal, GND ≤ V_W ≤ V_{DD}.
2	ADO	Programmable Pin 0 for Multiple Package Decoding. State is registered on power-up.
3	AD1	Programmable Pin 1 for Multiple Package Decoding. State is registered on power-up.
4	SDA	Serial Data Input/Output.
5	SCL	Serial Clock Input. Positive edge triggered.
6	V_{LOGIC}	Logic Power Supply.
7	GND	Digital Ground.
8	V_{DD}	Positive Power Supply.
9	B	B Terminal, GND ≤ V_B ≤ V_{DD}.
10	A	A Terminal, GND ≤ V_A ≤ V_{DD}.

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TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = V_{LOGIC} = 5.5 V, R_{AB} = 10 kΩ, T_A = +25°C; unless otherwise noted.

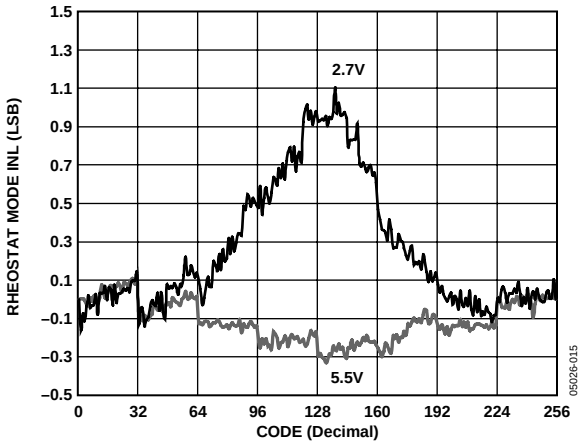

Figure 6. R-INL vs. Code vs. Supply Voltage

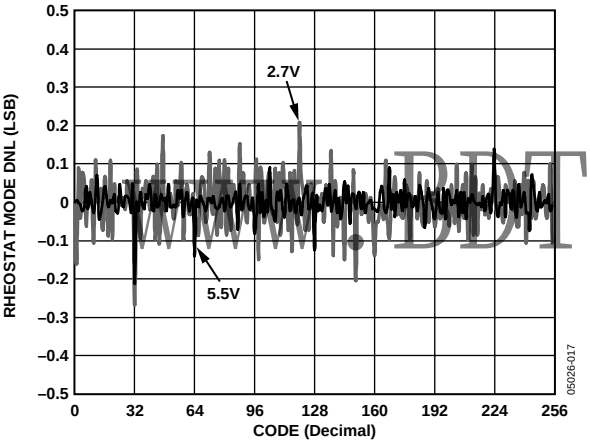

Figure 7. R-DNL vs. Code vs. Supply Voltage

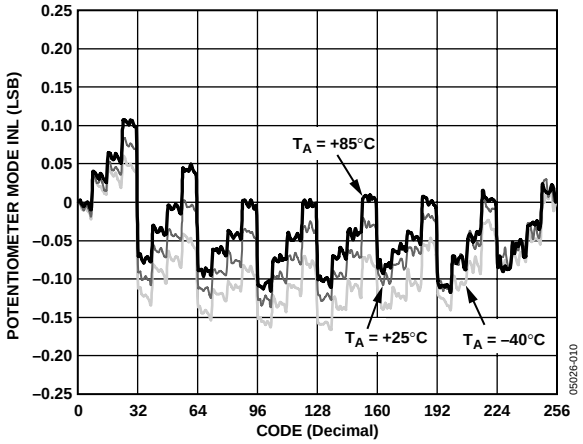

Figure 8. INL vs. Code vs. Temperature

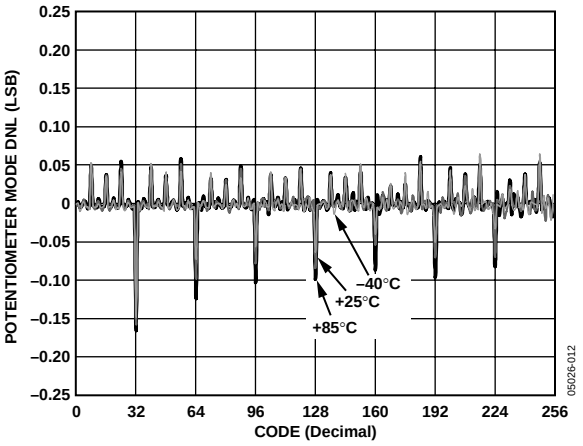

Figure 9. DNL vs. Code vs. Temperature

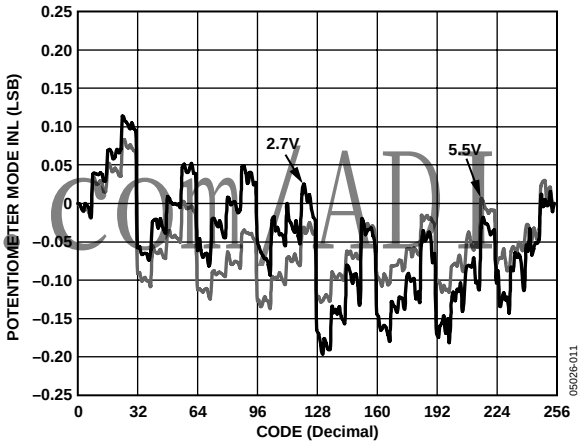

Figure 10. INL vs. Supply Voltages

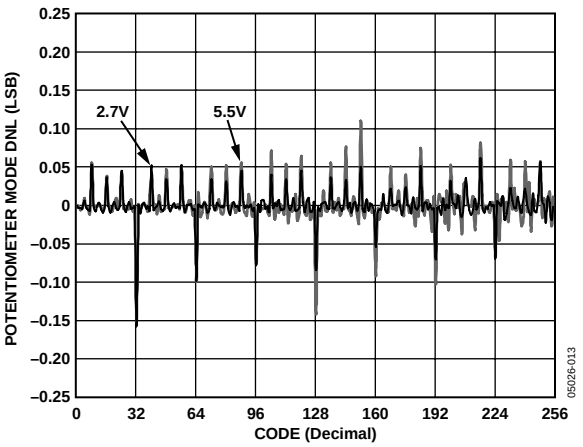

Figure 11. DNL vs. Code vs. Supply Voltage

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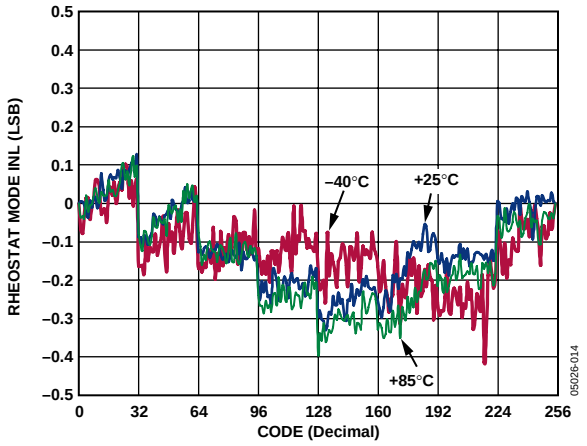

Figure 12. R-INL vs. Code vs. Temperature

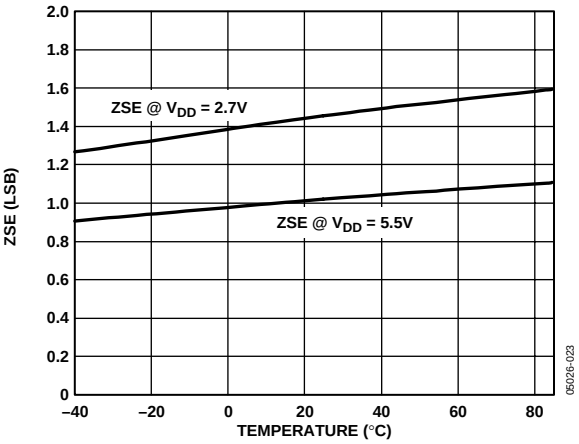

Figure 15. Zero-Scale Error vs. Temperature

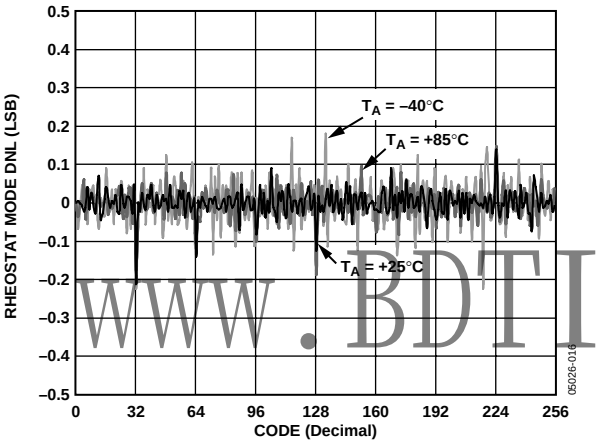

Figure 13. R-DNL vs. Code vs. Temperature

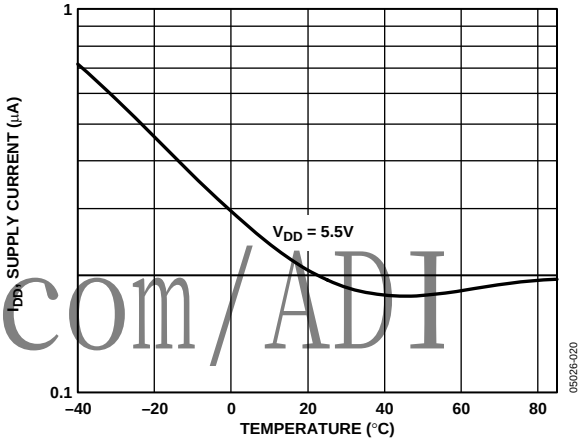

Figure 16. Supply Current vs. Temperature

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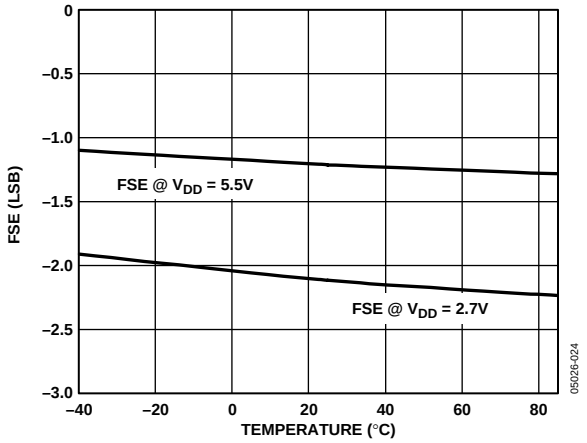

Figure 14. Full-Scale Error vs. Temperature

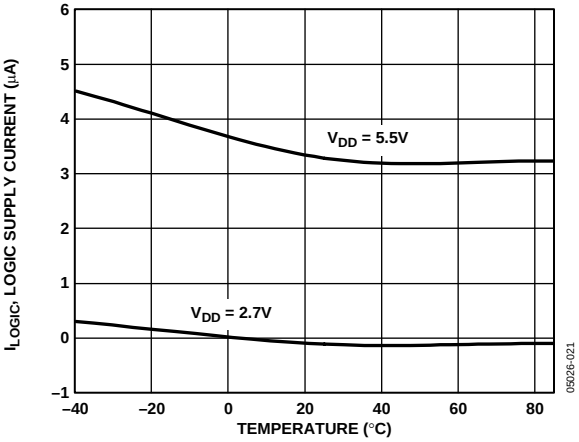

Figure 17. Logic Supply Current vs. Temperature vs. V_{DD}

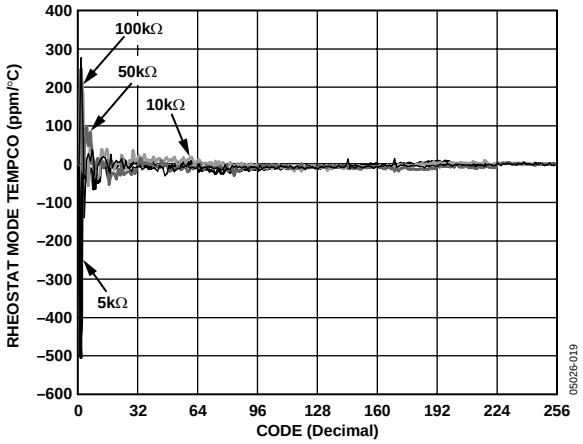

Figure 18. Rheostat Mode Tempco ($\Delta R_{AB} \times 10^6$)/($R_{AB} \times \Delta T$) vs. Code

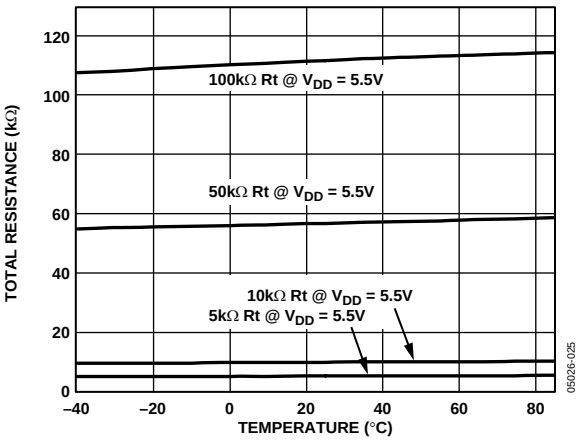

Figure 21. Total Resistance vs. Temperature

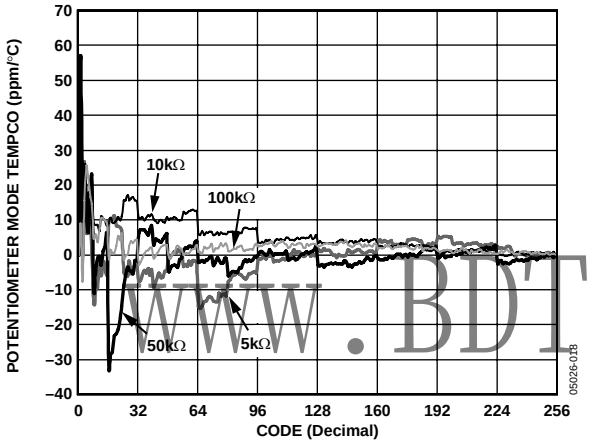

Figure 19. Potentiometer Mode Tempco ($\Delta V_W \times 10^6$)/($V_W \times \Delta T$) vs. Code

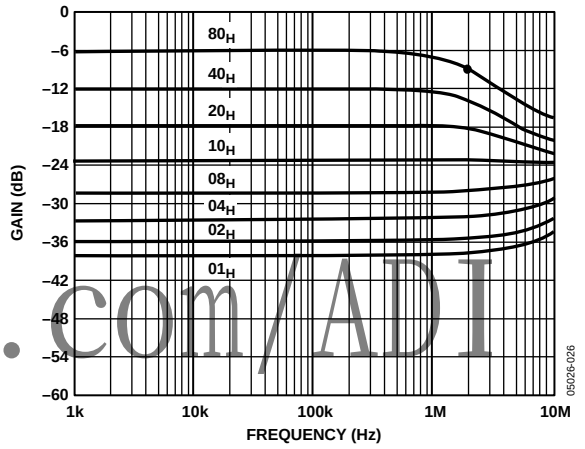

Figure 22. Gain vs. Frequency vs. Code, R_{AB} = 5 kΩ

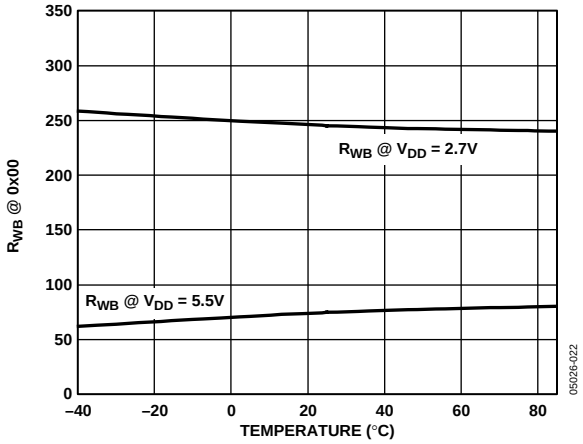

Figure 20. R_{WB} vs. Temperature

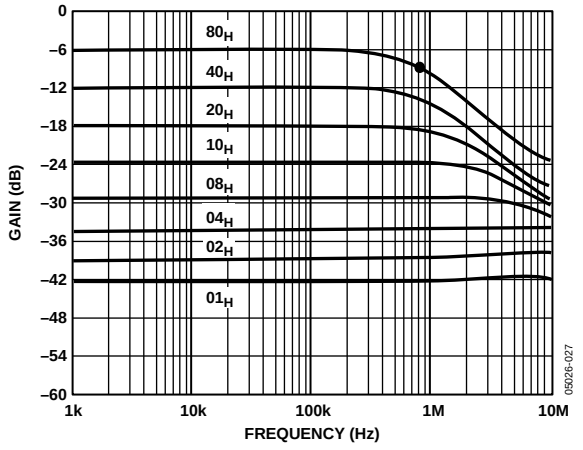

Figure 23. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

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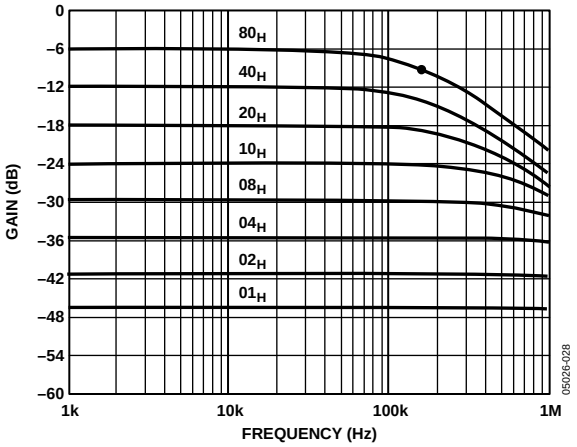

Figure 24. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

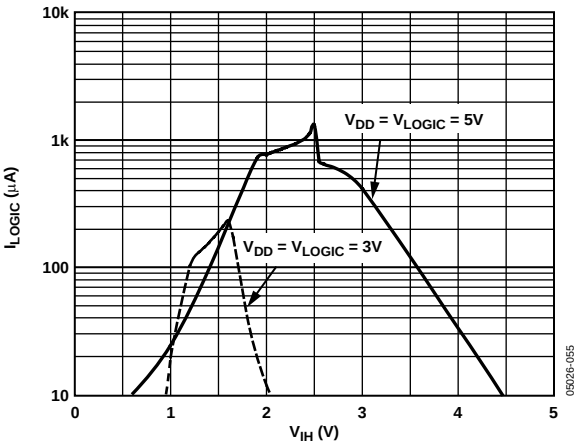

Figure 27. Logic Supply Current vs. Input Voltage

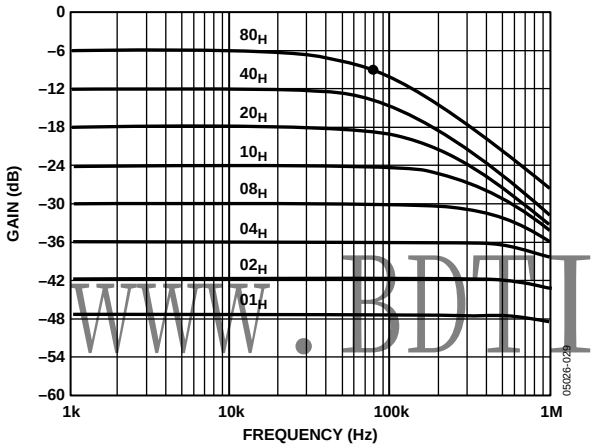

Figure 25. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

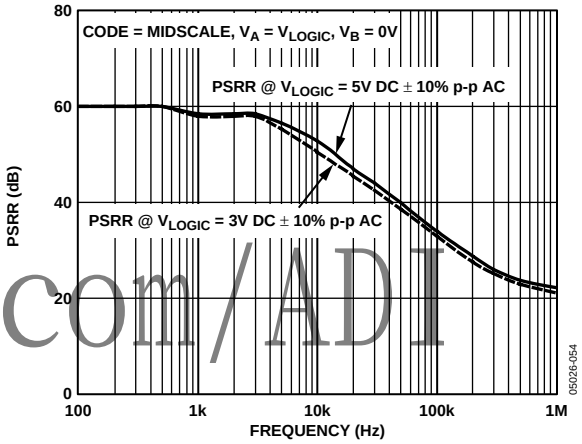

Figure 28. PSRR vs. Frequency

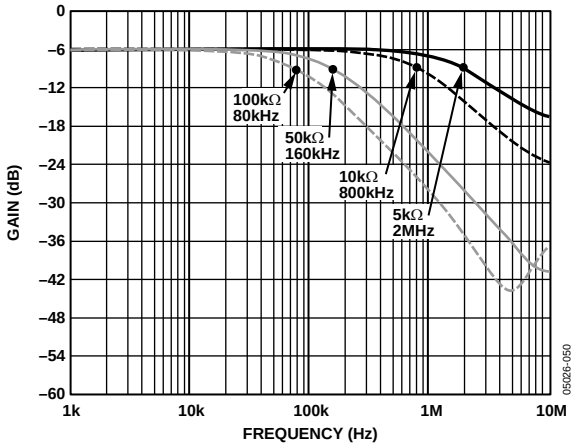

Figure 26. −3 dB Bandwidth @ Code = 0×80

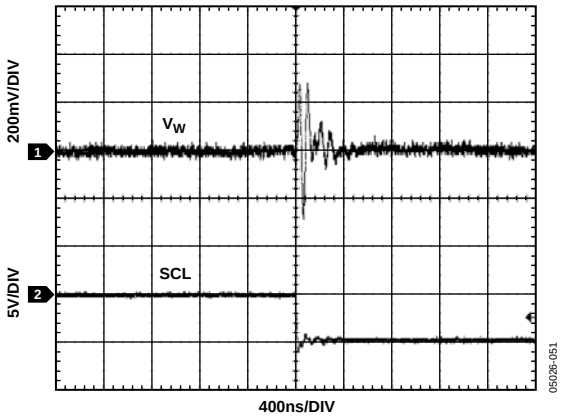

Figure 29. Digital Feedthrough

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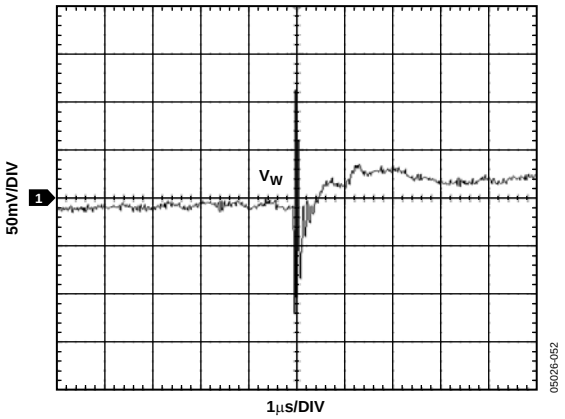

Figure 30. Midscale Glitch, Code 0×7F to 0×80

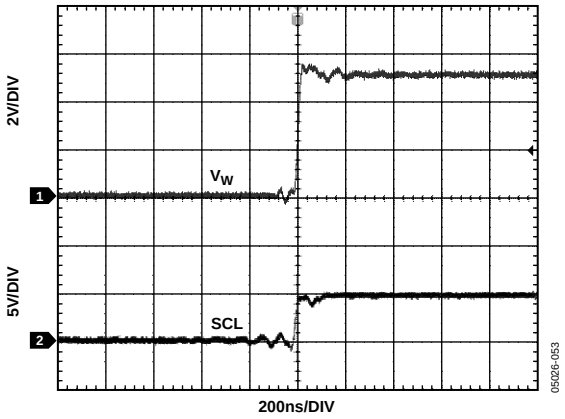

Figure 31. Large Signal Settling Time

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TEST CIRCUITS

Figure 32 through Figure 37 illustrate the test circuits that define the test conditions used in the product Specifications tables.

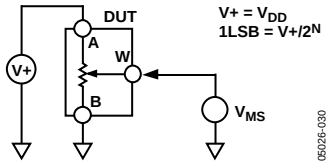

Figure 32. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

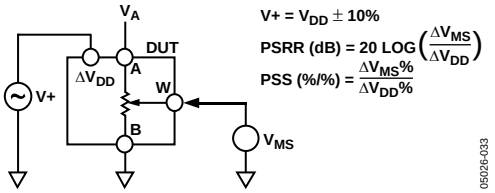

Figure 35. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

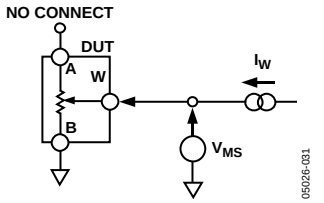

Figure 33. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

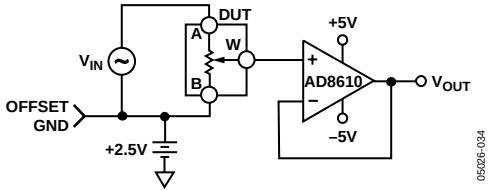

Figure 36. Test Circuit for Gain vs. Frequency

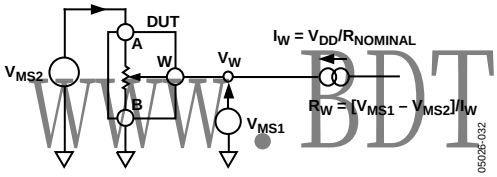

Figure 34. Test Circuit for Wiper Resistance

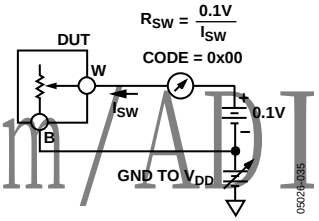

Figure 37. Test Circuit for Common-Mode Leakage Current

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THEORY OF OPERATION

The AD5259 is a 256-position digitally-controlled variable resistor (VR) device. EEPROM is pre-loaded at midscale from the factory, and initial power-up is, accordingly, at midscale.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance (R_{AB}) of the RDAC between Terminal A and Terminal B is available in 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The nominal resistance of the VR has 256 contact points accessed by the wiper terminal. The 8-bit data in the RDAC latch is decoded to select one of 256 possible settings.

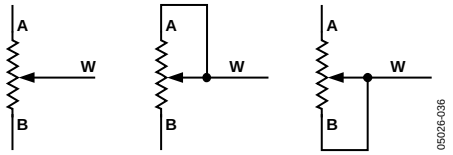

Figure 38. Rheostat Mode Configuration

The general equation determining the digitally programmed output resistance between Wiper W and Terminal B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the ON resistance of each internal switch.

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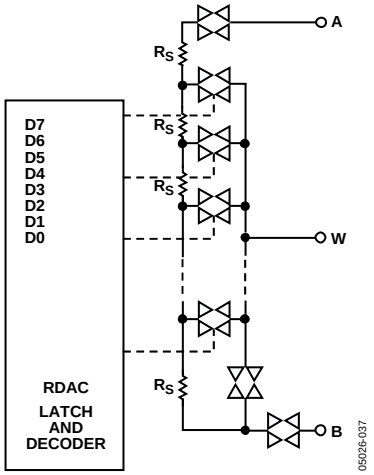

Figure 39. AD5259 Equivalent RDAC Circuit

In the zero-scale condition, there is a relatively low value finite wiper resistance. Care should be taken to limit the current flow between Wiper W and Terminal B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A produces a digitally controlled complementary resistance, R_{WA}. The resistance value setting for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

Typical device-to-device matching is process lot dependent and may vary by up to ±30%. For this reason, resistance tolerance is stored in the EEPROM, enabling the user to know the actual R_{AB} within 0.1%.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at Wiper W to Terminal B and Wiper W to Terminal A proportional to the input voltage at Terminal A to Terminal B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across Terminal A to Terminal B, Wiper W to Terminal A, and Wiper W to Terminal B can be at either polarity.

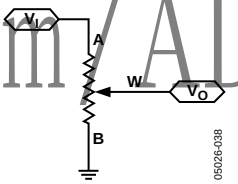

Figure 40. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at Wiper W to Terminal B starting at 0 V up to 1 LSB less than 5 V. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (3)$$

A more accurate calculation, which includes the effect of wiper resistance, V_W, is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the Internal Resistors R_{WA} and R_{WB} and not the absolute values.

I²C-COMPATIBLE INTERFACE

The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 4). The next byte is the slave address byte, which consists of the slave address (first 7 bits) followed by an R/$\overline{W}$ bit (see Table 6). When the R/$\overline{W}$ bit is high, the master reads from the slave device. When the R/$\overline{W}$ bit is low, the master writes to the slave device.

The slave address of the part is determined by two configurable address pins, Pin AD0 and Pin AD1. The state of these two pins is registered upon power-up and decoded into a corresponding I²C 7-bit address (see Table 5). The slave address corresponding to the transmitted address bits responds by pulling the SDA line low during the ninth clock pulse (this is termed the slave acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its serial register.

WRITING

In the write mode, the last bit (R/$\overline{W}$) of the slave address byte is logic low. The second byte is the instruction byte. The first three bits of the instruction byte are the command bits (see Table 6). The user must choose whether to write to the RDAC register, EEPROM register, or activate the software write protect (see Table 7 to Table 10). The final five bits are all zeros (see Table 13 to Table 14). The slave again responds by pulling the SDA line low during the ninth clock pulse.

The final byte is the data byte MSB first. With the write protect mode, data is not stored; rather, a logic high in the LSB enables write protect. Likewise, a logic low disables write protect. The slave again responds by pulling the SDA line low during the ninth clock pulse.

STORING/RESTORING

In this mode, only the address and instruction bytes are necessary. The last bit (R/$\overline{W}$) of the address byte is logic low. The first three bits of the instruction byte are the command bits (see Table 6). The two choices are transfer data from RDAC to EEPROM (store), or from EEPROM to RDAC (restore). The final five bits are all zeros (see Table 13 to Table 14).

READING

Assuming the register of interest was not just written to, it is necessary to write a dummy address and instruction byte. The instruction byte will vary depending on whether the data that is wanted is the RDAC register, EEPROM register, or tolerance register (see Table 11 and Table 16).

After the dummy address and instruction bytes are sent, a repeat start is necessary. After the repeat start, another address byte is needed, except this time the R/$\overline{W}$ bit is logic high. Following this address byte is the readback byte containing the information requested in the instruction byte. Read bits appear on the negative edges of the clock.

The tolerance register can be read back individually (see Table 15) or consecutively (see Table 16). Refer to the Read Modes section for detailed information on the interpretation of the tolerance bytes.

After all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition (see Figure 46). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, and then raises SDA high to establish a stop condition (see Figure 47).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output is updated on each successive byte until a stop condition is received. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

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I²C-COMPATIBLE FORMAT

The following generic, write, read, and store/restore control registers for the AD5259 all refer to the device addresses listed in Table 5; the mode/condition reference key (S, P, SA, MA, NA, $\overline{W}$, R, and X) is listed below.

S = Start Condition

P = Stop Condition

SA = Slave Acknowledge

MA = Master Acknowledge

NA = No Acknowledge

$\overline{\mathbf{W}}$ = Write

R = Read

X = Don't Care

AD1 and AD0 are two-state address pins.

Table 5. Device Address Lookup

AD1 Address Pin	AD0 Address Pin	I²C Device Address
0	0	0011000
1	0	0011010
0	1	1001100
1	1	1001110

GENERIC INTERFACE

Table 6. Generic Interface Format

S	**7-Bit Device Address** (See Table 5)	R/$\overline{W}$	SA	C2	C1	C0	A4	A3	A2	A1	A0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte									Data Byte									

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Table 7. RDAC-to-EEPROM Interface Command Descriptions

C2	C1	C0	Command Description
0	0	0	Operation Between Interface and RDAC.
0	0	1	Operation Between Interface and EEPROM.
0	1	0	Operation Between Interface and Write Protection Register. See Table 10.
1	0	0	NOP.
1	0	1	Restore EEPROM to RDAC.
1	1	0	Store RDAC to EEPROM.

WRITE MODES

Table 8. Writing to RDAC Register

S	**7-Bit Device Address** (See Table 5)	0	SA	0	0	0	0	0	0	0	0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte									Data Byte									

Table 9. Writing to EEPROM Register

S	**7-Bit Device Address** (See Table 5)	0	SA	0	0	1	0	0	0	0	0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte									Data Byte									

Table 10. Activating/Deactivating Software Write Protect

S	**7-Bit Device Address** (See Table 5)	0	SA	0	1	0	0	0	0	0	0	SA	0	0	0	0	0	0	0	WP	SA	P
	Slave Address Byte			Instruction Byte									Data Byte									

In order to activate the write protection mode, the WP bit in Table 10 must be logic high. To deactivate the write protection, the command must be sent again, except with the WP in logic zero state. WP is reset to the deactivated mode if power is cycled off and on.

READ MODES

Read modes are referred to as traditional because the first two bytes for all three cases are dummy bytes, which function to place the pointer towards the correct register; this is the reason for the repeat start. Theoretically, this step can be avoided if the user reads a register previously written to. For example, if the EEPROM was just written to, the user can then skip the two dummy bytes and proceed directly to the slave address byte, followed by the EEPROM readback data.

Table 11. Traditional Readback of RDAC Register Value

S	**7-Bit Device Address** (See Table 5)	0	SA	0	0	0	0	0	0	0	0	SA	S	**7-Bit Device Address** (See Table 5)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte			Instruction Byte										Slave Address Byte			Read Back Data									

↑

Repeat start

Table 12. Traditional Readback of Stored EEPROM Value

S	**7-Bit Device Address** (See Table 5)	0	SA	0	0	1	0	0	0	0	0	SA	S	**7-Bit Device Address** (See Table 5)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte			Instruction Byte										Slave Address Byte			Read Back Data									

↑

Repeat start

STORE/RESTORE MODES

Table 13. Storing RDAC Value to EEPROM

S	**7-Bit Device Address** (See Table 5)	0	SA	1	1	0	0	0	0	0	0	SA	P
	Slave Address Byte			Instruction Byte									

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Table 14. Restoring EEPROM to RDAC

S	**7-Bit Device Address** (See Table 5)	0	SA	1	0	1	0	0	0	0	0	SA	P
	Slave Address Byte			Instruction Byte									

TOLERANCE READBACK MODES

Table 15. Traditional Readback of Tolerance (Individually)

| | | |

ESD PROTECTION OF DIGITAL PINS AND RESISTOR TERMINALS

The AD5259 V_{DD}, V_{LOGIC}, and GND power supplies define the boundary conditions for proper 3-terminal and digital input operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V_{DD} or GND are clamped by the internal forward biased ESD protection diodes (see Figure 42). Digital Input SCL and Digital Input SDA are clamped by ESD protection diodes with respect to V_{LOGIC} and GND as shown in Figure 43.

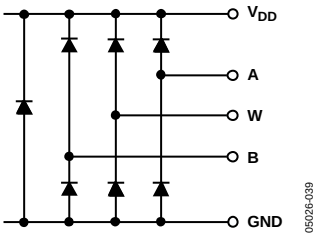

Figure 42. Maximum Terminal Voltages Set by V_{DD} and GND

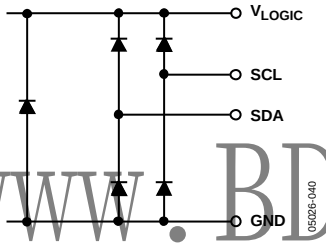

Figure 43. Maximum Terminal Voltages Set by V_{LOGIC} and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 42), it is important to power GND/V_{DD}/V_{LOGIC} before applying any voltage to Terminal A, Terminal B, and Terminal W; otherwise, the diode is forward biased, so the V_{DD} and V_{LOGIC} are powered unintentionally and may affect the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, V_{LOGIC}, digital inputs, and then V_A, V_B, V_W. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after GND/V_{DD}/V_{LOGIC}.

LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to use compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 44). The digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

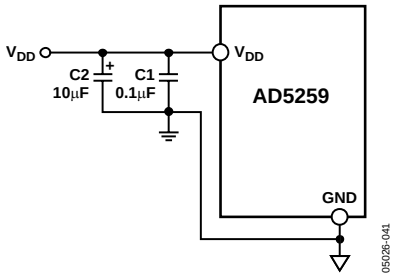

Figure 44. Power Supply Bypassing

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MULTIPLE DEVICES ON ONE BUS

The AD5259 has two configurable address pins, Pin AD0 and Pin AD1. The state of these two pins is registered upon power-up and decoded into a corresponding I^2C-compatible 7-bit address (see Table 5). This allows up to four devices on the bus to be written to or read from independently.

EVALUATION BOARD

An evaluation board, with all necessary software, is available to program the AD5259 from any PC running Windows® 98/ 2000/ XP. The graphical user interface, as shown in Figure 45, is straightforward and easy to use. More detailed information is available in the board's user manual.

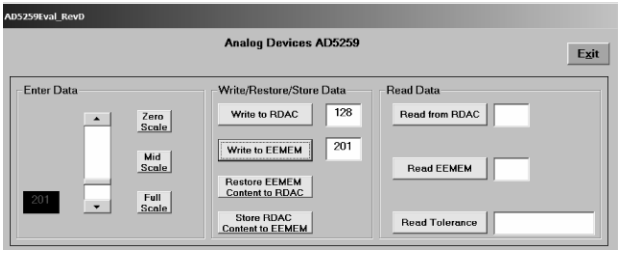

Figure 45. AD5259 Evaluation Board Software

DISPLAY APPLICATIONS

CIRCUITRY

A special feature of the AD5259 is its unique separation of the V_{LOGIC} and V_{DD} supply pins. The separation provides greater flexibility in applications that do not always provide needed supply voltages.

In particular, LCD panels often require a V_{COM} voltage in the range of 3 V to 5 V. The circuit in Figure 46 is the rare exception in which a 5 V supply is available to power the digital potentiometer.

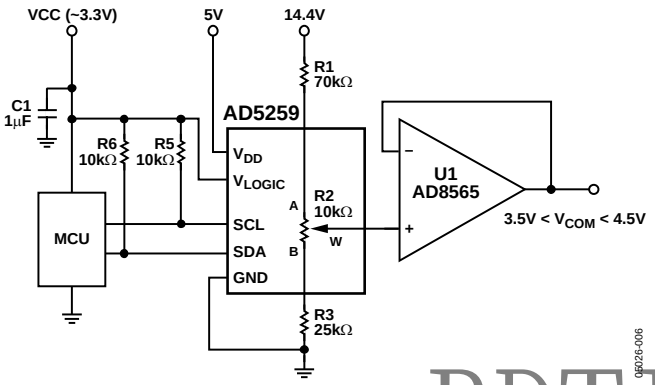

Figure 46. V_{COM} Adjustment Application

In the more common case shown in Figure 47, only analog 14.4 V and digital logic 3.3 V supplies are available. By placing discrete resistors above and below the digital potentiometer, V_{DD} can now be tapped off the resistor string itself. Based on the chosen resistor values, the voltage at V_{DD} in this case equals 4.8 V, allowing the wiper to be safely operated all the way up to 4.8 V. The current draw of V_{DD} will not affect that node's bias because it is only on the order of microamps. V_{LOGIC} is tied to the MCU's 3.3 V digital supply because V_{LOGIC} will draw the 35 mA which is needed when writing to the EEPROM. It would be impractical to try and source 35 mA through the 70 kΩ resistor, therefore, V_{LOGIC} is not connected to the same node as V_{DD}.

For this reason, V_{LOGIC} and V_{DD} are provided as two separate supply pins that can either be tied together or treated independently; V_{LOGIC} supplying the logic/EEPROM with power, and V_{DD} biasing up the A, B, and W terminals for added flexibility.

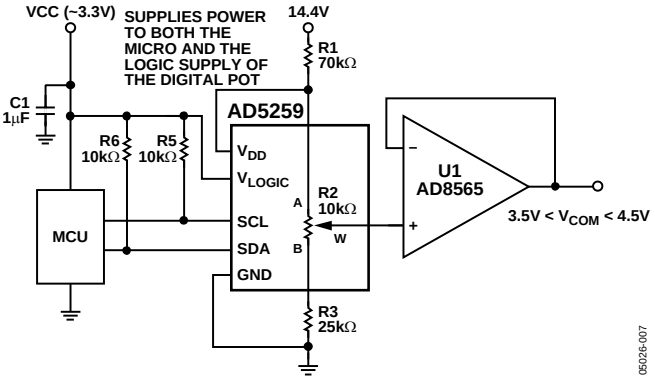

Figure 47. Circuitry When a Separate Supply is Not Available for V_{DD}

For a more detailed look at this application, refer to the article, "Simple VCOM Adjustment uses any Logic Supply Voltage" in the September 30, 2004 issue of *EDN* magazine.

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OUTLINE DIMENSIONS

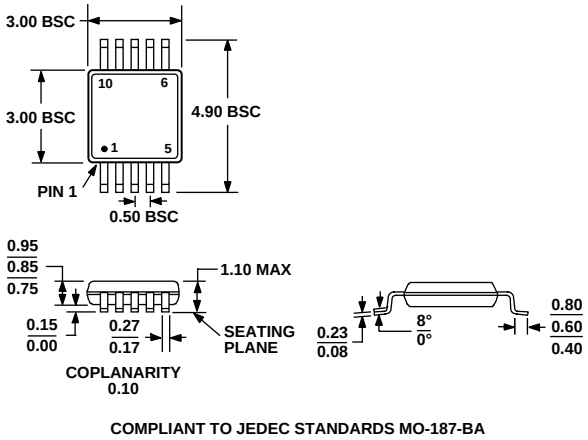

Figure 48. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

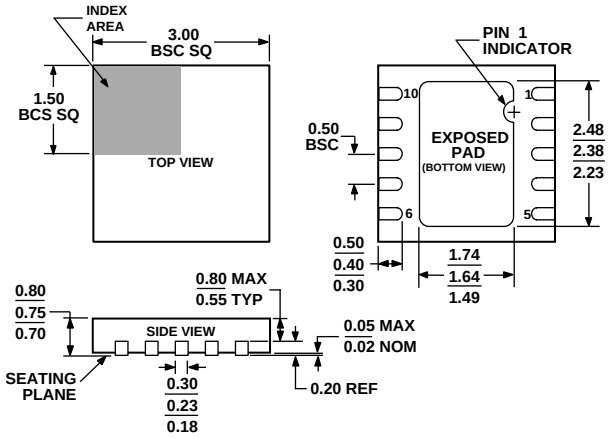

Figure 49. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]

3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (Ω)	Temperature	Package Description	Package Option	Branding
AD5259BRMZ5[1]	5 k	–40°C to +85°C	10-Lead MSOP	RM-10	D4P
AD5259BRMZ5-R7[1]	5 k	–40°C to +85°C	10-Lead MSOP	RM-10	D4P
AD5259BCPZ5-R7[1]	5 k	–40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	D4P
AD5259BRMZ10[1]	10 k	–40°C to +85°C	10-Lead MSOP	RM-10	D4Q
AD5259BRMZ10-R7[1]	10 k	–40°C to +85°C	10-Lead MSOP	RM-10	D4Q
AD5259BCPZ10-R7[1]	10 k	–40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	D4Q
AD5259BRMZ50[1]	50 k	–40°C to +85°C	10-Lead MSOP	RM-10	D4R
AD5259BRMZ50-R7[1]	50 k	–40°C to +85°C	10-Lead MSOP	RM-10	D4R
AD5259BCPZ50-R7[1]	50 k	–40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	D4R
AD5259BRMZ100[1]	100 k	–40°C to +85°C	10-Lead MSOP	RM-10	D4S
AD5259BRMZ100-R7[1]	100 k	–40°C to +85°C	10-Lead MSOP	RM-10	D4S
AD5259BCPZ100-R7[1]	100 k	–40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	D4S
AD5259EVAL[2]			Evaluation Board		

[1] Z = Pb-free part.
[2] The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

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